Remarks

This application has been reviewed in light of the Office Action dated October 11, 2006. In view of this amendment, Claims 1, 3, 8-11, 13-18, 20, 21, 31, and 32 are now pending in this case, with Claims 1, 7-11, 13-15, 18, 20, and 21 being amended. Claim 7 has been cancelled. Claims 33-35 have been added. Applicants petition for a two-month (2) extension of time.

THE OBJECTION TO CLAIM 20

Claim 20 was objected to for lack of antecedent basis for the limitation "the component" in line 9. Claim 20 has been amended at line 7 to recite "**a** component of **a** back illuminated imager" so that "the component" in line 9 has antecedent basis to "a component" in line 7. Accordingly, withdrawal of the objection to claim 20 is respectfully requested.

THE 35 U.S.C. 112, SECOND PARAGRAPH REJECTION

Claims 1, 3, 7-11, 13-15 and 18 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as their invention.

Claims 1, 7, and 11 were rejected because the Examiner was unclear as to what happens "in response to a bias potential applied to the at least two gate electrodes." Claims 1 and 11 have been amended to refer to " said charge wells being formed in response to a bias potential applied to the at least two gate electrodes." Claims 1, 11, and 18 were rejected because

the Examiner viewed as unclear how an interelectrode gap can be located in the substrate. Claims 1, 11, and 18 have been amended to refer to the "at least two gate electrodes being separated by an inter-electrode gap between the at least two gate electrodes." Claims 1, 11, and 18 were rejected because the Examiner viewed as unclear how a semiconductor region can be viewed as an apparatus. This rejection is rendered moot in light of the amendments to claims 1, 11, and 18 which remove the reference to an apparatus. Claims 11 and 13 were rejected because claim 11 refers to a "photo-gate optical sensor" and claim 13 refers only to a "photogate." The Examiners views it as unclear whether "photogate" refers to the "photogate optical sensor." Claims 11 and 13 have been amended to refer to photo-gate optical sensor at all positions where "photogate" previously appeared. The Examiner rejected claims 9 and 14 based on the statement in these claims of "the further well region forming a further charge barrier well." In the view of the Examiner, it is unclear how a well region can form another well region and what does it structurally mean. The Examiner also rejected claims 9 and 14 because it is unclear to the Examiner how a plurality of diffusion regions can form one charge sink. Applicants have amended claims 9 and 14 to refer to a second diffusion region of the second conductivity type in the further charge barrier well, the second diffusion region forming a charge sink. Because of Applicants amendments to claims 1, 9, 11, 13, 14, and 11 set forth above, Applicants respectfully request the withdrawal of the 35 U.S.C. §112, second paragraph rejection of claims 1, 3, 7-11, 13-15 and 18.

THE 35 U.S.C. 112, SECOND AND FOURTH PARAGRAPH REJECTION

Claim 21 stand rejected under 35 U.S.C. §112, second and fourth paragraph, as not further limiting an imager according to one of claims 18 and 20. Applicants have amended claim 21 to refer to claims 18 only, and further to limit claim 21 to refer to a charge coupled device further comprising optics that are configured to focus radiation onto the back side of the substrate. Because of Applicants amendments to claim 21 set forth above, Applicants respectfully request the withdrawal of the 35 U.S.C. §112, second paragraph and fourth paragraph rejection of claim 21.

THE 35 U.S.C. 102(B) REJECTION OF CLAIM 20

Claim 20 stands rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,875,084 (herein "Tohyama") .

In the Office Action, the Examiner states that Tohyama, in FIG. 8, teaches providing a back illuminated imager comprising a substrate (21), a photodetector (24), a well region (26), the well region and the substrate forming a semiconductor junction; and at least one diffusion region (30), whereby the component of the back illuminated imager is shielded from photocarriers by the semiconductor junction (junction between 21 and 26 of FIG. 8). However, Applicants respectfully submit that Tohyama fails to disclose each and every element of Claim 20 as amended. Specifically, Tohyama does not disclose a CCD pixel structure overlying at least one diffusion region, as cited in amended claim 20. Photoelectric converting region (24), while capable detecting light in conjunction with potential-barrier region (25), the carrier injected

region (22), the guard ring (26) and the silicon dioxide layer (27), such a structure does not form a structure consistent with CCD pixel structures known in the art. CCD pixel structures generally have at least two gates overlying diffusion regions, one gate for accumulating charge, and one gate for transferring the accumulated charge through the diffusion region. Tohyama, in contrast, has a single monolithic photoelectric converting region (24). Accordingly, because Tohyama fails to disclose each and every element of amended Claim 20, the §103(a) rejection of Claims 20 should be withdrawn.

THE 35 U.S.C. §103(A) REJECTION OF CLAIMS 1, 7-11, 13-15, 31 AND 32

Claims 1, 7-11, 13-15, 31 and 32 stand rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 4,995,061 (herein "Hynecek") in view of U.S. Patent No. 6,465,820 (herein "Fox").

In the Office Action, the Examiner states that Hynecek, in FIG. 1a, teaches a charge coupled device made on a substrate (10), the charge coupled device comprising: a dielectric layer (18) overlying at least a portion of the substrate (10), at least two gate electrodes (20, 22) overlying the dielectric layer (18), the at least two gate electrodes configured to define at least two charge wells (14, 16), the at least two gate electrodes separated by an interelectrode gap (between gates (20) and (22).

The Examiner states that a means for stabilizing the interelectrode gap includes applying respective bias potentials to the two gate electrodes (20 and 22), the bias potential being sufficient to cause a fringing field to extend across the interelectrode gap from at least one of the at least two gate electrodes. In contrast, claims 1 and 11, as amended, recite a means for

stabilizing the interelectrode gap includes a semiconductor region of the first conductivity type, formed in the interelectrode gap, but having a different dopant concentration than the substrate. This semiconductor regions is illustrated as the inserted semiconductor regions 414 of FIG. 4A, 466 of FIG. 4C, and 494 of FIG. 4D. The region (23) of Hynecek lying between the two gate electrodes (20 and 22) is a virtual gate having the purpose and function of aiding in the transfer of charge between the gate electrodes (20 and 22). Furthermore, Hynecek discloses additional structures (26 and 30), which virtual gate (23) overlies in the interelectrode gap of FIG. 1a. Structure (26) is a virtual well for accumulating charge, while structure (30) is a virtual barrier region. Both structures (26) and (30), along with clocked barrier region (16) together constitute a second phase region (38), i.e., a portion of a CCD pixel structure(see column 5, lines 6-17 of Hynecek). Hynecek does not teach or suggest that any of virtual gate (23), virtual well (26), or virtual barrier region (30), has the effect of stabilizing the interelectrode gap. .As such, Applicants respectfully submit that Hynecek fails to disclose each and every element of claim 1 and 11 as amended. The rejection of claim 7 is moot in view of its cancellation.

Fox fails to correct the deficiencies of Hynecek. Fox discloses diode sub-region (32) and (36) of FIG. 1a, functioning with underlying diode sub-region (34) form an overall diode (30) as part of an overall CCD pixel structure. Like Hycenek, Fox does not teach or suggest that diode structure (30) stabilizes the interelectrode gap. As such, Applicants respectfully submit that Fox fails to disclose each and every element of claim 1 and 11 as amended.

Therefore, neither Hynecek, nor Fox, alone or in combination, teach or suggest the invention as claimed in independent claims 1 or 11, and claims 3, 8-10, 13-15, 31 and 32, dependent therefrom. For at least the reasons set forth above, Applicants respectfully request the

withdrawal of the 35 U.S.C. §103(a) rejection based on Hynecek in view of Fox for Claims 1, 8-11, 13-15, 31 and 32.

THE 35 U.S.C. §103(A) REJECTION OF CLAIM 3

Claim 3 stands rejected under 35 U.S.C. § 103(a) as obvious over a combination of the following references: Hynecek., Fox, and U.S. Patent No. 5,210,433 ("Ohsawa et al.").

Ohsawa fails to correct the deficiencies of Hynecek . Referring to FIG. 3 of Oshawa, Ohsawa discloses photodiodes 14 in a gap bridged by metal thin film layers 30 and 32 which function together with photodiode 14 as a CCD pixel structure. Phototodiode 14 has the purpose of collecting charge from incident light. Like Hycenek and Fox, Ohsawa does not teach or suggest that photodiode 14 stabilizes an interelectrode gap. As such, Applicants respectfully submit that Oshawa fails to disclose each and every element of claim 1 and 11 as amended, and claim 3 dependent therefrom.

Therefore, neither Hynecek, Fox, nor Oshawa, alone or in combination, teach or suggest the invention as claimed in independent claims 1, and claim 3 dependent therefrom. For at least the reasons set forth above, Applicants respectfully request the withdrawal of the 35 U.S.C. §103(a) rejection based on Hynecek in view of Fox in view of Oshawa for Claim 3.

THE 35 U.S.C. §103(A) REJECTION OF CLAIM 18

Claim 18 stands rejected under 35 U.S.C. § 103(a) as obvious over a combination of U. S. Patent No 4,952,523 ("Fujii") in view of Fox.

In the Office Action, the Examiner states that Fujii teaches a substrate (10), a well region (32); an oxide layer (12) formed over at least the well region (32); first (42) and second (44)

electrodes formed of polysilicon on the oxide layer (12), and first (42) and second (44) gate electrodes being separated by an inter-electrode gap (the gap between 42 and 44), wherein the combination of the first and second polysilicon gate electrodes, the oxide layer and the well region form a buried channel CCD register and means for stabilizing the interelectrode gap.

The Examiner states that a means for stabilizing the interelectrode gap includes applying respective bias potentials to the two gate electrodes (42 and 44), the bias potential being sufficient to cause a fringing field to extend across the interelectrode gap from at least one of the at least two gate electrodes. In contrast, claims 1 and 11, as amended, recite a means for stabilizing the interelectrode gap includes a semiconductor region of the second conductivity type, formed in the inter-electrode gap of the well region for stabilizing the inter-electrode gap, but having a different dopant concentration than the well region. This semiconductor regions is illustrated as the inserted semiconductor regions 414 of FIG. 4A, 466 of FIG. 4C, and 494 of FIG. 4D. The regions (34, 36, 38) of Fujii lying between the two gate electrodes (42 and 44) are virtual electrode regions which for, along with gates (42) and (44), form a buried channel CCD structure. Hynecek does not teach or suggest that regions (34, 36, 38) stabilize the interelectrode gap. .As such, Applicants respectfully submit that Fujii fails to disclose each and every element of claim 18 as amended.

Fox fails to correct the deficiencies of Hynecek as discussed above for claims 1, 3, and 11. Fox discloses diode sub-region (32) and (36) of FIG. 1a, functioning with underlying diode sub-region (34) form an overall diode (30) as part of an overall CCD pixel structure. As such, Applicants respectfully submit that Fox fails to disclose each and every element of claim 18 as amended.

Therefore, neither Fujii, nor Fox, alone or in combination, teach or suggest the invention as claimed in independent claims 18, and claims 33-35, dependent therefrom. For at least the reasons set forth above, Applicants respectfully request the withdrawal of the 35 U.S.C. §103(a) rejection based on Fujii in view of Fox for Claim 18, and allowance of claims 33-35.

THE 35 U.S.C. §103(A) REJECTION OF CLAIMS 16 AND 17

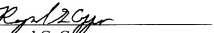
Claims 16 and 17 stand rejected under 35 U.S.C. § 103(a) as obvious over a combination of U. S. Patent No 6,088,057 ("Hieda") in view of Fujii. Fujii discloses a CCD imager array on a single monolithic circuit. Heida discloses digitization circuit (3) separate from a CCD circuit (2) (See FIG. 1). The digitization circuit 3 in FIG 2 of Heida consists of sample-and-hold circuits 10, 11, a switch circuit 12, a clamp-type amplifier 13, an A/D converter 14, and a voltage reference source 15 which are formed on one IC (see column 3, lines 29-30). The CCD (2) is not formed on the same IC as the digitization circuit 3. Since claim 16 calls for a single monolithic circuit on which both a CCD and A/D converter are formed, then neither Heida nor Fujii, alone or in combination, teaches or suggests each and every element of claim 16. Claim 17 also teaches a single monolithic circuit on which both a CCD and A/D converter are formed. As such, neither Heida nor Fujii, alone or in combination, teaches or suggests each and every element of claim 17. For at least the reasons set forth above, Applicants respectfully request the withdrawal of the 35 U.S.C. §103(a) rejection based on Heida in view of Fujii for claim 16 and 17.

THE 35 U.S.C. §103(A) REJECTION OF CLAIM 21

Claim 21 stands rejected under 35 U.S.C. § 103(a) as obvious over a combination of Tohyama in view of U. S. Patent No 6,489,992 ("Savoye"). Claim 21 has been amended to be depended from claim 18. Old claim 21 was rejected based on claim 21 being depended from claim 20. For reasons discussed above for Claim 18, Tohyama fails to teach each and every element of claim 21, namely a means for stabilizing the interelectrode gap includes a semiconductor region of the second conductivity type, formed in the inter-electrode gap of the well region for stabilizing the inter-electrode gap, but having a different dopant concentration than the well region, as cited in amended claim 18. Savoye fails to cure the deficiencies of Tohyama. Savoye recites a standard back illuminated CCD device coupled with imaging optics to form a CCD imaging system. There is no teaching or suggestion in Savoye that the CCD device employed in the system has a semiconductor region of the second conductivity type, formed in the inter-electrode gap of the well region for stabilizing the inter-electrode gap, but having a different dopant concentration than the well region. As such, neither Tohyama nor Savoye, alone or in combination, teaches or suggests each and every element of claim 21. For at least the reasons set forth above, Applicants respectfully request the withdrawal of the 35 U.S.C. §103(a) rejection based on Tohyama in view of Savoye for claim 21.

In view of the foregoing remarks, Applicants respectfully request favorable reconsideration and an early allowance of the claims pending in the present application.

A $600.00 is believed to be due for a two (2) month extension of time and three (3) new claims in connection with the present Amendment. If, however, other fees are deemed necessary for this Amendment to be entered and considered by the Examiner, then the Commissioner is authorized to charge such fee to Deposit Account No. 501358. Applicants' undersigned attorney may be reached by telephone at (973) 597-2500. All correspondence should continue to be directed to our address listed below.



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